REMARKS

The Examiner is thanked for the careful examination of the application.

The Examiner has rejected all of the pending claims under 35 U.S.C. § 103 based upon the Wahbe and Honcik references, or in combination with the Applicant's admitted prior art.

The Applicant respectfully suggests that all of the claims, as amended, are patentable in view of the cited references. Furthermore, the Applicant believes that the Wahbe and Honcik references fail to establish a *prima facie* case of obviousness with respect to the claims, as amended.

When examining a claim for obviousness, each and every limitation of the claims must be fully considered. To fail to fully consider a single claim limitation is a failure to consider the claim as a whole, as is required by §103.

Claim 1 includes limitations to a first *native instruction set;* it further contains limitations to a *predetermined subset of said first set of native instructions.* It further includes limitations to a *first virtual machine instruction set which includes said first set of native instructions, except for said first predetermined subset....*

The Wahbe reference teaches a mechanism for protecting the system against malicious software. His focus is on restricting the software to a generic memory protection model that sandboxes the memory space of the software.

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The present invention teaches protecting the software from a "malicious" system
(processor). Our focus is on restricting the virtual machine to a *restricted subset of
the underlying processor*, thus sandboxing the functionality of the VM implementation.

Wahbe's virtual machine does not purport to protect against faults in the generic
processor; his purpose is to protect against faults in the user software. The Examiner
appears to agree when saying that Wahbe speaks of "general purpose of global
pointers".

Wahbe speaks of instructions that are likely to result in defects when executed.
However, as the Examiner points out (paragraph 1, Page 3 of the office action), Wahbe
is referring to instructions in the virtual machine instruction set. When we discuss
instructions likely to expose defects, we are referring to instructions in the native
instruction set of the underlying processor.

Additionally, Wahbe suggests abstracting away from the underlying hardware (p2
20-25). We teach a strict analysis of the features of the underlying hardware employed
by the VM.

When you appreciate the quantity and character of the differences between
Wahbe and the present invention, it becomes clear that there are no teachings, nor any
suggestions, that Wahbe somehow be modified or changed to apply to differences in
the NATIVE instruction set. When there are not even any suggestions in the cited
references to modify or change the cited references to arrive at the claimed
combination, it becomes clear that the references fail to establish a *prima facie* case of
obviousness.

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With respect to claim 19, the cited references fail to establish a *prima facie* case of obviousness with respect to the claimed method. There is no teaching in the cited references that one would even think of attempting to gain acceptance by the FAA of the dual processors configured as claimed. The Examiner would need to find an example of an FAA certification of a similar type of equipment. The Applicant believes that there is no teaching that would even suggest one to try to obtain approval of such a design. The Applicant believes that such designs have not been implemented in the FAA environment, despite the need for high assurances for many years. It is improper hindsight to say it would be obvious when the Examiner can find not a single example of a similar architecture being used in an FAA environment.

The Applicant believes that the application and claims, as amended, are in condition for allowance, and early notification of the same would be much appreciated.

Respectfully submitted,

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